Abstract

A system for communication on a chip. The system includes an on-chip communication bus including plural tracks, and a plurality of stations that couple a plurality of on-chip components to the on-chip communication bus, whereby the plurality of on-chip components use the tracks to communicate. Each station preferably includes an initiator that requests permission to transmit outgoing data over a track to another station and that transmits the outgoing data, an arbiter that evaluates requests from other stations and selects a track on which to receive incoming data, and a target that receives the incoming data. The initiator can be connected to a grant multiplexor for selecting a grant line, with the grant multiplexor further including plural smaller multiplexors distributed across the chip. Likewise, the arbiter can be connected to a track multiplexor for selecting a track, with the track multiplexor further including plural smaller multiplexors distributed across the chip. Each station also can include a source queue for queuing outgoing data and a destination queue for queuing incoming data. Preferably, the queues are first-in-first-out registers. The source queue and the destination queue can serve to separate a first clock domain for the on-chip communication bus from a second clock domain for one of the plurality of on-chip components. More than one of the plurality of on-chip components can be coupled to the on-chip communication bus through one of the stations.